LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A magnetic memory device comprising:

a magneto-resistance effect element including a magnetic sensitive layer whose magnetization direction changes according to an external magnetic field;

a write line to which a write current is supplied to apply the external magnetic field to the magnetic sensitive layer; and

a write current drive circuit including a current direction control section configured to control ~~for controlling~~ the direction of the write current in said write line and a current amount control section configured to control ~~for controlling~~ the amount of the write current in said write line to a constant value.

2. (Currently Amended) The magnetic memory device as claimed in claim 1 wherein the current direction control section is configured to select ~~selects~~ one of both ends of said write line to which current is to be supplied as an inflow side of the write current and the other as an outflow side, thereby controlling the direction of the write current.

3. (Currently Amended) The magnetic memory device as claimed in claim 2 wherein the current direction control section is configured to bidirectionally control ~~controls~~ the direction of the write current in response to an input write data signal.

4. (Original) The magnetic memory device as claimed in claim 2, wherein said write line is connected at both ends to the write current drive circuit.

5. (Original) The magnetic memory device as claimed in claim 4, wherein said write line has a closed loop shape.

6. (Currently Amended) The magnetic memory device as claimed in claim 4, wherein the current direction control section comprises:

a first differential switch pair comprising a first current switch and a second current switch being provided corresponding to both ends of said write line and configured to operate ~~for operating~~ so as to become an opposite open/closed state to each other; and

a second differential switch pair comprising a third current switch and a fourth current switch being provided corresponding to the first current switch and the second current switch and configured to operate ~~for operating~~ so as to become an opposite open/closed state to each other, and

wherein the first differential switch pair has a function of selecting one of both ends of said write line as the inflow side of the write current and the second differential switch pair has a function of selecting the other as the outflow side of the write current.

7. (Original) The magnetic memory device as claimed in claim 6, wherein the first current switch and the fourth current switch operate so as to become the same open/closed state, and

wherein the second current switch and the third current switch operate so as to become the opposite open/closed state to that of the first and fourth current switches.

8. (Currently Amended) The magnetic memory device as claimed in claim 6, wherein at least either the first or second differential switch pair is configured to perform ~~performs~~ open/closed operation in response to the data signal.

9. (Original) The magnetic memory device as claimed in claim 6, wherein both ends of said write line are connected to a pair of joint points between the first and second differential switch pairs.

10. (Original) The magnetic memory device as claimed in claim 6, wherein the current direction control section comprises differential control means for controlling so that the first current switch and the fourth current switch become the same open/closed state and the second current switch and the third current switch become the opposite open/closed state to that of the first and fourth current switches.

11. (Original) The magnetic memory device as claimed in claim 10 wherein the differential control means detects the open/closed state of one of the first and second differential switch pairs and controls the open/closed operation of the other based on the detection result.

12. (Original) The magnetic memory device as claimed in claim 10, wherein the differential control means comprises a fifth current switch and a sixth current switch for operating so as to become the opposite open/closed state to each other.

13. (Original) The magnetic memory device as claimed in claim 12, wherein the fifth current switch detects the open/closed state of the third current switch and causes the second current switch to operate so as to become the same open/closed state as the third current switch, and

wherein the sixth current switch detects the open/closed state of the fourth current switch and causes the first current switch to operate so as to become the same open/closed state as the fourth current switch.

14. (Original) The magnetic memory device as claimed in claim 6, wherein the first to fourth current switches are implemented as first to fourth transistors.

15. (Original) The magnetic memory device as claimed in claim 12, wherein the first to fourth current switches are implemented as first to fourth transistors.

16. (Original) The magnetic memory device as claimed in claim 14, wherein said write line is connected at one end to an emitter of the first transistor and a collector of the third transistor and at an opposite end to an emitter of the second transistor and a collector of the fourth transistor.

17. (Original) The magnetic memory device as claimed in claim 16, wherein collectors of the first and second transistors are connected to a power supply.

18. (Original) The magnetic memory device as claimed in claim 14, wherein one of the third and fourth transistors of the second differential switch pair has a base to which a write data signal is input and the other has a base to which a signal provided by inverting the data signal is input.

19. (Original) The magnetic memory device as claimed in claim 15, wherein the fifth and sixth current switches are implemented as fifth and sixth transistors.

20. (Original) The magnetic memory device as claimed in claim 19, wherein the fifth and sixth transistors have bases connected to the collectors of the third and fourth transistors and have collectors to which bases of the second and first transistors are connected.

21. (Currently Amended) The magnetic memory device as claimed in claim 19, wherein the write current drive circuit comprises a seventh transistor functioning as a switch configured to operate ~~for operating~~ the write current drive circuit and a first current limiting resistor, and

wherein the seventh transistor has a collector to which emitters of the fifth and sixth transistors are connected in common and has an emitter grounded through the first current limiting resistor.

22. (Original) The magnetic memory device as claimed in claim 19, wherein a first bias resistor is provided between the connection point of the collector of the fifth transistor and the base of the second transistor and a power supply and a second bias resistor is provided between the connection point of the collector of the sixth transistor and the base of the first transistor and the power supply.

23. (Original) The magnetic memory device as claimed in claim 22, wherein the first and second transistors have characteristics matched, the third and fourth transistors have characteristics matched, the fifth and sixth transistors have characteristics matched, and the first and second bias resistors have characteristics matched.

24. (Original) The magnetic memory device as claimed in claim 1, wherein the current amount control section is provided on the path of the write current flowing out from said write line.

25. (Original) The magnetic memory device as claimed in claim 14, wherein the current amount control section comprises at least an eighth transistor and a second current limiting resistor, and

wherein the eighth transistor has a collector connected to emitters of the third and fourth transistors in common, has an emitter grounded through the second current limiting resistor, and has a base to which a constant voltage is input selectively.

26. (Currently Amended) The magnetic memory device as claimed in claim 25 wherein the constant voltage is an active signal for the write current drive circuit and the eighth transistor also functions as a switch for causing the write current drive circuit to operate in response to the active signal.

27. (Currently Amended) The magnetic memory device as claimed in claim 19, wherein the write current drive circuit comprises a seventh transistor functioning as a switch configured to operate ~~for operating~~ the write current drive circuit and a first current limiting resistor and the seventh transistor has a collector to which emitters of the fifth and sixth transistors are connected in common and has an emitter grounded through the first current limiting resistor,

wherein a first bias resistor is provided between the connection point of the collector of the fifth transistor and the base of the second transistor and a power supply and a second

bias resistor is provided between the connection point of the collector of the sixth transistor and the base of the first transistor and the power supply,

the current amount control section comprises at least an eighth transistor and a second current limiting resistor and the eighth transistor has a collector connected to emitters of the third and fourth transistors in common, has an emitter grounded through the second current limiting resistor, and has a base to which a constant voltage is input selectively, and

wherein the first to eighth transistors, the first and second bias resistors, and the first and second current limiting resistors are all integrated in the same area.

28. (Original) The magnetic memory device as claimed in claim 1, wherein the magneto-resistance effect element comprises: a layered product comprising the magnetic sensitive layer and configured so that a current flows in a perpendicular direction to the deposition face; and

a toroidal magnetic layer being disposed on one face of the layered product so that the direction along the deposition face is an axial direction and penetrated by said write line.

29. (Original) The magnetic memory device as claimed in claim 28 wherein said write line comprises a plurality of first write lines and a plurality of second write lines extended so as to cross the plurality of first write lines, and

wherein the first and second write lines are extended in parallel with each other in the area penetrating the toroidal magnetic layer.

30. (Original) The magnetic memory device as claimed in claim 1, wherein one storage cell comprises a pair of the magneto-resistance effect elements.

31. (Original) The magnetic memory device as claimed in claim 30 wherein the magnetization directions of the magnetic sensitive layers in the pair of the magneto-resistance effect elements change so as to become antiparallel with each other according to magnetic fields induced to currents flowing through the first and second write lines and information is stored in the storage cell.

32. (Currently Amended) A write current drive circuit applied to a magnetic memory device comprising a magneto-resistance effect element comprising a magnetic sensitive layer whose magnetization direction changes according to an external magnetic field and a write line to which a write current is supplied to apply an external magnetic field to the magnetic sensitive layer, said write current drive circuit comprising:

a pair of connection ends to which both ends of the write line are connected;

a current direction control section configured to control ~~for controlling~~ the direction of the write current in the write line; and

a current amount control section configured to control ~~for controlling~~ the amount of the write current allowed to flow into the write line to a constant value.

33. (Currently Amended) The write current drive circuit as claimed in claim 32 wherein said current direction control section comprises:

a first differential switch pair comprising a first current switch and a second current switch being provided corresponding to both ends of the write line for operating so as to become an opposite open/closed state to each other;

a second differential switch pair comprising a third current switch and a fourth current switch being provided corresponding to the first current switch and the second current switch

configured to operate ~~for operating~~ so as to become an opposite open/closed state to each other; and

differential control means for controlling so that the first current switch and the fourth current switch become the same open/closed state and the second current switch and the third current switch become the opposite open/closed state to that of the first and fourth current switches.

34. (Original) The write current drive circuit as claimed in claim 33, wherein the first to fourth current switches are implemented as first to fourth transistors.

35. (Original) The write current drive circuit as claimed in claim 34, wherein the write line is connected at one end to an emitter of the first transistor and a collector of the third transistor and at an opposite end to an emitter of the second transistor and a collector of the fourth transistor.

36. (Original) The write current drive circuit as claimed in claim 32, wherein said current amount control section comprises a transistor having a base to which a constant voltage is input and a current limiting resistor and is provided on the path of the write current flowing out from the write line.

37. (Original) A write current drive method applied to a magnetic memory device comprising a magneto-resistance effect element comprising a magnetic sensitive layer whose magnetization direction changes according to an external magnetic field and a write line to which a write current is supplied to apply an external magnetic field to the magnetic sensitive layer, said write current drive method comprising the steps of:

selecting one of both ends of the write line to which current is to be supplied as an inflow side of the write current and the other as an outflow side, thereby controlling the direction of the write current; and

supplying the write current while controlling so that the write current flows on the write line in a constant current value.

38. (Currently Amended) The write current drive method as claimed in claim 37 comprising the steps of:

providing a first differential switch pair comprising a first transistor and a second transistor being provided corresponding to both ends of the write line for operating so as to become an opposite open/closed state to each other;

providing a second differential switch pair comprising a third transistor and a fourth transistor being provided corresponding to the first transistor and the second transistor for operating so as to become an opposite open/closed state to each other; and

providing differential control means for controlling so that the first transistor and the fourth transistor become the same open/closed state and the second transistor and the third transistor become the opposite open/closed state to that of the first and fourth transistors;

connecting the write line at one end to an emitter of the first transistor and a collector of the third transistor and at an opposite end to an emitter of the second transistor and a collector of the fourth transistor;

bidirectionally switching the direction of the write current allowed to flow into the write line; providing a current amount control section comprising a transistor having a base to which a constant voltage is input and a current limiting resistor on the path of the write current flowing out from the write line; and

controlling the amount of the write current in the write line to a constant value.

39. (Original) The write current drive method as claimed in claim 38, wherein the third and fourth transistors are caused to perform open/closed operation in response to the direction in which the write current is allowed to flow into the write line, whereby the second differential switch pair selects one end of the write line as an outflow side of the write current, wherein

the differential control means detects the open/closed state of each transistor of the second differential switch pair and controls the operation of the second transistor so as to become the same open/closed state as the third transistor and the operation of the first transistor so as to become the same open/closed state as the fourth transistor, and wherein

the first and second transistors perform open/closed operation, whereby the first differential switch pair selects the other end of the write line as an inflow side of the write current.